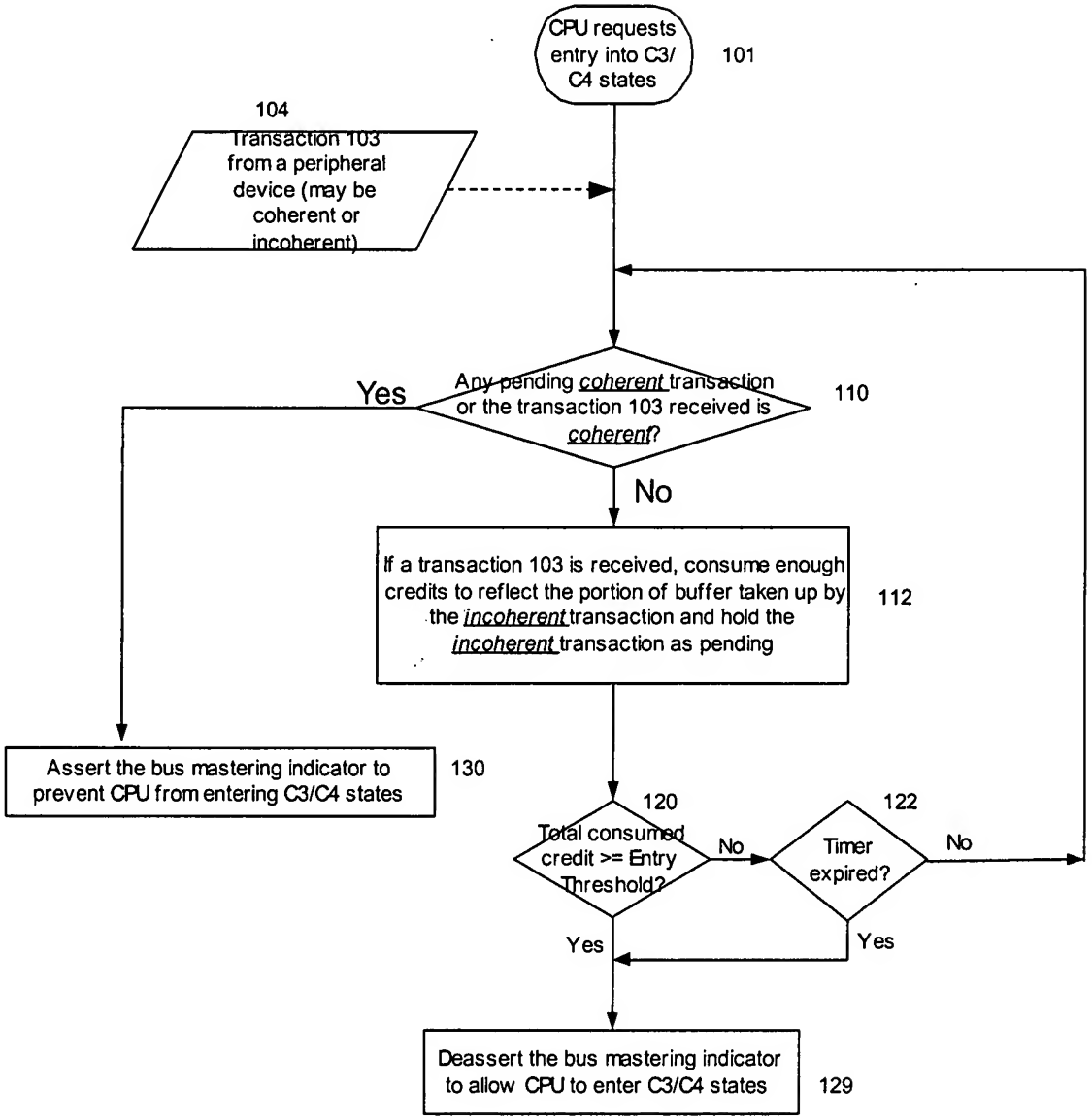

CPU requests entry into C3/ C4 states
101
104
Transaction 103 from a peripheral device (may be coherent or incoherent)
Yes
Any pending coherent transaction or the transaction 103 received is coherent?
110
No
If a transaction 103 is received, consume enough credits to reflect the portion of buffer taken up by the incoherent transaction and hold the incoherent transaction as pending
112
Assert the bus mastering indicator to prevent CPU from entering C3/C4 states
130
120
Total consumed credit >= Entry Threshold?
No
122
Timer expired?
No
Yes
Yes
Deassert the bus mastering indicator to allow CPU to enter C3/C4 states
129

Figure 1A

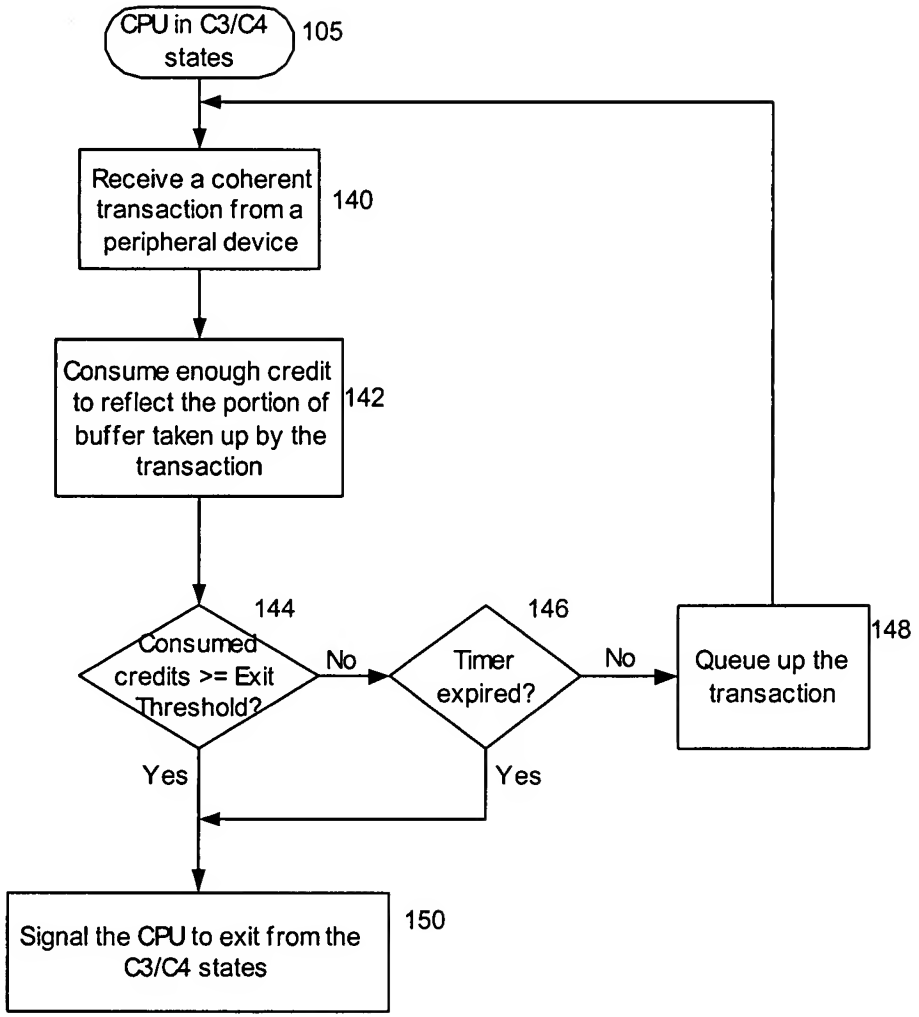
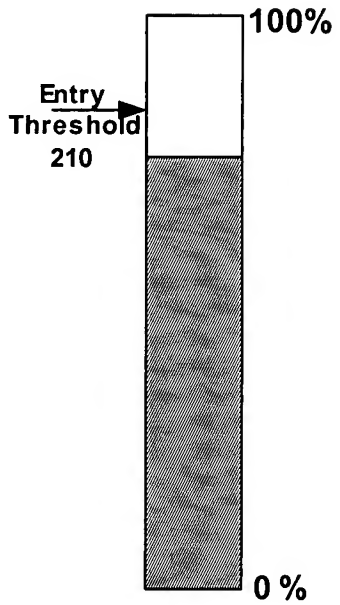
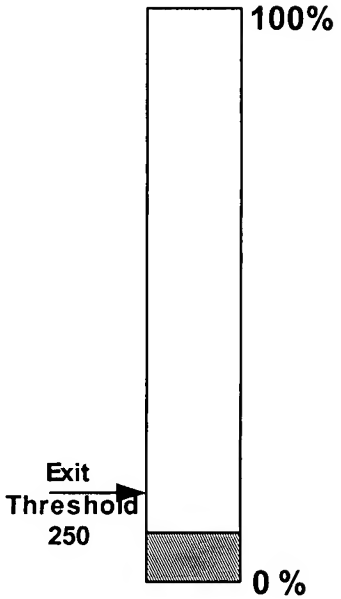

CPU in C3/C4 states
105
Receive a coherent transaction from a peripheral device
140
Consume enough credit to reflect the portion of buffer taken up by the transaction
142
144
Consumed credits >= Exit Threshold?
No
146
Timer expired?
No
148
Queue up the transaction
Yes
Yes
Signal the CPU to exit from the C3/C4 states
150

Figure 1B



Flow control credit setting for C3/C4 Entry

Figure 2A



Flow control credit setting for C3/C4 exit

Figure 2B

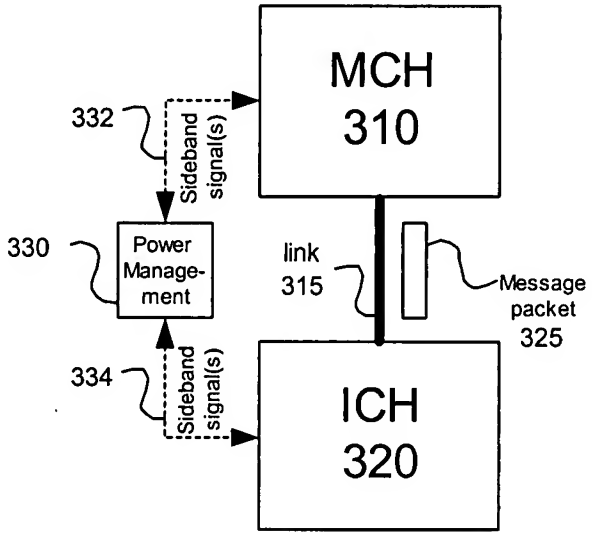


Figure 3A

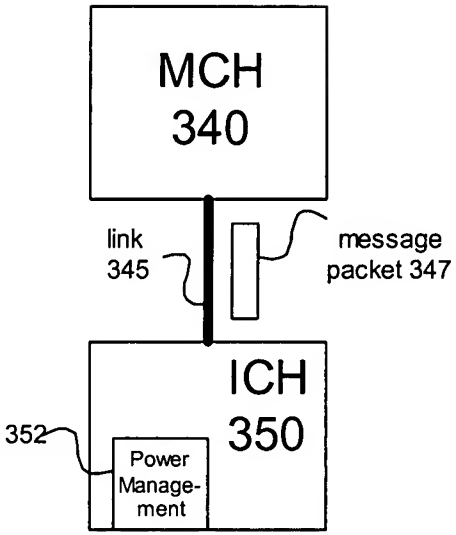


Figure 3B

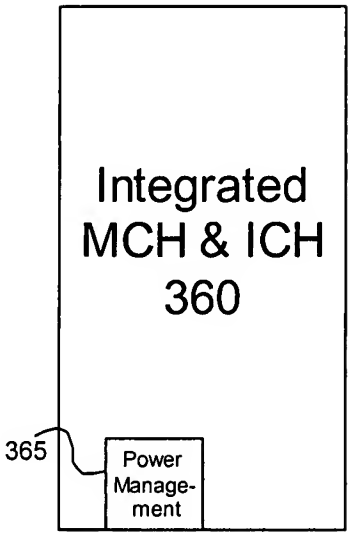


Figure 3C

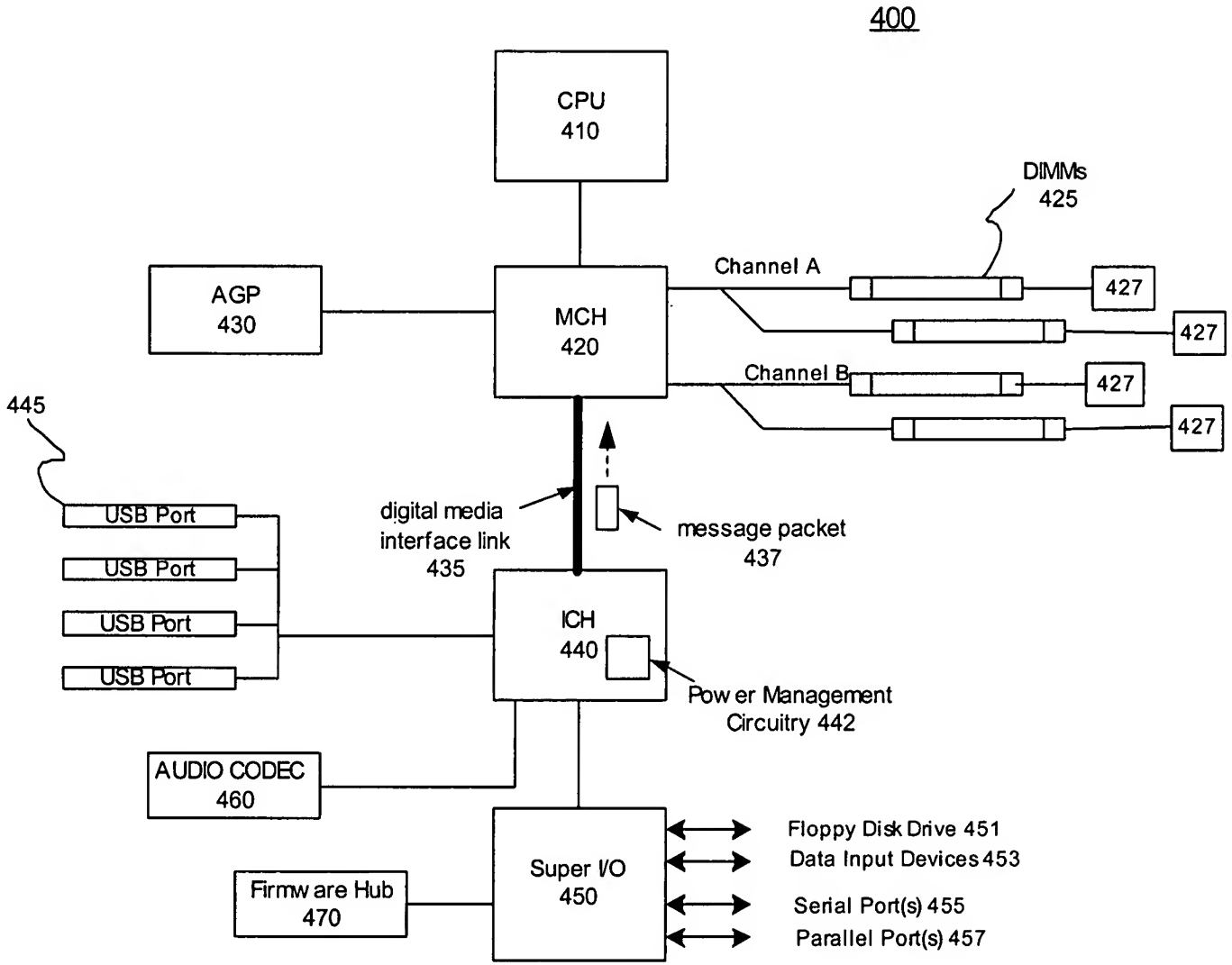

400
CPU
410
DIMMs
425
AGP
430
MCH
420
Channel A
427
427
Channel B
427
427
445
USB Port
USB Port
USB Port
USB Port
digital media
interface link
435
message packet
437
ICH
440
Power Management
Circuitry 442
AUDIO CODEC
460
Super I/O
450
Floppy Disk Drive 451
Data Input Devices 453
Serial Port(s) 455
Parallel Port(s) 457
Firmware Hub
470

Figure 4